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1 Proactive process-level live migration in HPC environments

Chao Wang, Frank Mueller, Christian Engelmann, Stephen L. Scott

November 2008 SC '08: Proceedings of the 2008 ACM/IEEE conference on S

Publisher: IEEE Press

Full text available: Pdf (248.77 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 23, Downloads (12 Months): 45, Citation

As the number of nodes in high-performance computing environments k faults are becoming common place. Reactive fault tolerance (FT) often c due to massive I/O requirements and relies on manual job resubmissior

2 Proactive fault tolerance for HPC with Xen virtualization

Arun Babu Nagarajan, Frank Mueller, Christian Engelmann, Stephen L. Sco

June 2007 ICS '07: Proceedings of the 21st annual international conferenc Supercomputing

Publisher: ACM

Full text available: Pdf (526.85 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 24, Downloads (12 Months): 359, Citatio

Large-scale parallel computing is relying increasingly on clusters with th processors. At such large counts of compute nodes, faults are becoming Current techniques to tolerate faults focus on reactive schemes to recov

Keywords: high-performance computing, proactive fault tolerance, virt

3 Implementing the scale vector-thread processor

Ronny Krashinsky, Christopher Batten, Krste Asanović

July 2008 Transactions on Design Automation of Electronic Systems Volume 13 Issue 3

Publisher: ACM

Full text available: Pdf (11.74 MB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 93, Citation (

The Scale vector-thread processor is a complexity-effective solution for computing which flexibly supports both vector and highly multithreaded 7.1-million transistor chip has 16 decoupled execution clusters, vector l

Keywords: Vector processors, hybrid C++/Verilog simulation, iterative

flow, multithreaded processors, procedural datapath pre-placement, vec processors

4 High-performance ethernet-based communications for future multi-c
Michael Schlansker, Nagabhushan Chitlur, Erwin Oertli, Paul M. Stillwell, Jr Dennis Bradford, Richard J. Carter, Jayaram Mudigonda, Nathan Binkert, N
November 2007 SC '07: Proceedings of the 2007 ACM/IEEE conference on S
Publisher: ACM
Full text available: Pdf (540.15 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 22, Downloads (12 Months): 219, Citatio

Data centers and HPC clusters often incorporate specialized networking system requirements. However, Ethernet's low cost and high performan shift from specialized fabrics toward standard Ethernet. Although Etherr

5 FaCSim: a fast and cycle-accurate architecture simulator for embedc
Jaejin Lee, Junghyun Kim, Choonki Jang, Seungkyun Kim, Bernhard Egger, SangYong Han
June 2008 LCTES '08: Proceedings of the 2008 ACM SIGPLAN-SIGBED con Languages, compilers, and tools for embedded systems
Publisher: ACM
Full text available: Pdf (664.75 KB) Additional Information: full citation, abstract, referen

Bibliometrics: Downloads (6 Weeks): 28, Downloads (12 Months): 204, Citatio

There have been strong demands for a fast and cycle-accurate virtual p embedded systems area where developers can do meaningful software including performance debugging in the context of the entire platform. I

Keywords: architecture simulator, cycle-accurate simulation, full-syste simulator parallelization, virtual prototyping

Also published in:
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